4 Advanced Pipelining and Instruction-Level Parallelism

4.1 Instruction-Level Parallelism: Concepts and Challenges
4.2 Overcoming Data Hazards with Dynamic Scheduling
4.3 Reducing Branch Penalties with Dynamic Hardware Prediction
4.4 Taking Advantage of More ILP with Multiple Issue
4.5 Compiler Support for Exploiting ILP
4.6 Hardware Support for Extracting More Parallelism
4.7 Studies of ILP
4.8 Putting It All Together: The PowerPC 620
4.9 Fallacies and Pitfalls
4.10 Concluding Remarks
4.11 Historical Perspective and References
Exercises

5 Memory-Hierarchy Design

5.1 Introduction
5.2 The ABCs of Caches
5.3 Reducing Cache Misses
5.4 Reducing Cache Miss Penalty
5.5 Reducing Hit Time
5.6 Main Memory
5.7 Virtual Memory
5.8 Protection and Examples of Virtual Memory
5.9 Crosscutting Issues in the Design of Memory Hierarchies
5.10 Putting It All Together: The PowerPC 620
5.11 Fallacies and Pitfalls
5.12 Concluding Remarks
5.13 Historical Perspective and References
Exercises

6 Storage Systems

6.1 Introduction
6.2 Types of Storage Devices
6.3 Buses: Connecting I/O Devices to CPU/Memory
6.4 I/O Performance Measures
6.5 Reliability, Availability, and RAID
6.6 Crosscutting Issues: Interfacing to an Operating System
6.7 Designing an I/O System
6.8 Putting It All Together: UNIX File System Performance
6.9 Fallacies and Pitfalls
6.10 Concluding Remarks
6.11 Historical Perspective and References
Exercises

7 Interconnection Networks