

DÉMONSTRATION Nº 10

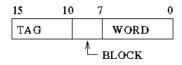
- Correction -

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Cache Memory

1. Determine the number of bits in the TAG, BLOCK, and WORD fields in main memory addresses.

Since no mention is made of bytes, assume the memory is word addressable. The main memory is 64K words, so an address is 16 bits. The block size is 128 words, so the WORD field is 7 bits. The cache size is 1K words, so there are 8 cache lines. (size of cache divided by size of block). Therefore, the BLOCK field is 3 bits. The remaining 6 bits is the TAG. Here's how an address is partitioned:



2. Compute the total time needed for instruction fetching during execution of the program.

On a hit, 1τ is spent fetching an instruction. On a miss, 128 words must be fetched from memory, so filling the cache line takes 1280τ time. I assume that the cache is *not* a load-through cache, so an additional 1τ time is spent transferring a word from the cache to the CPU.

Here's how the blocks fit into the cache:

Block		Tag
0	0-127	0
	1024-1151	1
1	128-255	0
	1152-1279	1
2	256-383	0
	1280-1407	1
3	384-511	0
	1408-1535	1
4	512-639	0
5	640-767	0
6	768-895	0
7	896-1023	0

Here's how execution proceeds:

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17-22: miss on 17

1st time through outer loop:
23-164: miss on 128
165-239: 20 times, no misses
240-1200: misses on 256, 384, 512, 640, 768, 896, 1024 (replacing 0-127), 1152 (replacing 128-255)

next 9 times through outer loop:
23-164: misses on 23 (replacing 1024-1151), 128 (replacing 1152-1279)
165-239: 20 times, no misses
240-1200: misses on 1024 (replacing 0-127), 1152 (replacing 128-255)

1201-1500: misses on 1280 (replacement), 1408 (replacement)
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Total cache fetches: 26,336 for **26,336** τ time. Total misses: 48 for miss penalty of **61,440** τ . Total time: **87,776** τ .