



DIRO  
IFT 1215

## DÉMONSTRATION N° 4

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Exercices tirés du livre de V.P. Heuring and H.F. Jordan  
**Computer Systems Design and Architecture, 1997.**

Photocopies distribuées en classe de démonstration

<b>Annexe 1</b>	<b>Circuits Combinatoires</b>
Exercices numéro ....	A.30
	<b>Circuits séquentiels &amp; FSM</b>
Exercices numéro ....	A.32, A.34, A.35, A.38

### A.32

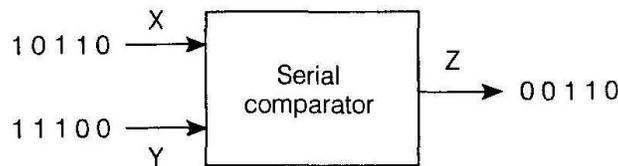
Create a state transition diagram for an FSM that sorts two binary words  $A$  and  $B$ , input serially with most significant bit first, onto two binary outputs  $GE$  and  $LT$ . If  $A$  is greater than or equal to  $B$ , then  $A$  appears on the  $GE$  line, and  $B$  appears on the  $LT$  line. If  $B$  is greater than  $A$ , then  $B$  appears on the  $GE$  line, and  $A$  appears on the  $LT$  line.

### A.34

Design an FSM that outputs a 1 when the last three inputs are 011 or 110. Just show the state table. Do not draw a circuit.

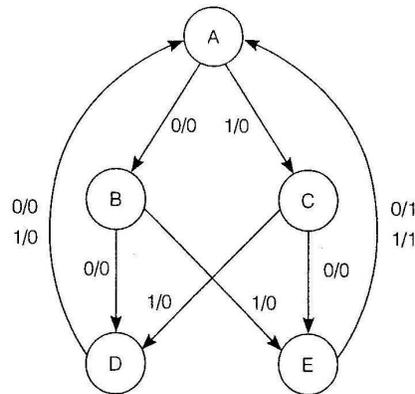
### A.35

Design a finite state machine that takes two binary words  $X$  and  $Y$  in serial form, least significant bit (LSB) first, and produces a 1-bit output  $Z$  that is true when  $X > Y$  and is 0 for  $X \leq Y$ . When the machine starts, assume that  $X = Y$ . That is,  $Z$  produces 0's until  $x > y$ . The diagram shows a sample input sequence and the corresponding output sequence.



### A.38

Given the state transition diagram shown below, do the following :



1. Create a state table.
2. Design a circuit for the state machine described by your state table, using D-flip-flop(s), a single decoder, and OR gates. For the state assignment, use the bit pattern that corresponds to the position of each letter in the alphabet, starting from 0. For example,  $A$  is at position 0, so the state assignment is 000;  $B$  is at position 1, so the state assignment is 001, and so on.