

Filtering Tricks for FSK Demodulation

In the past decades, economical implementations of digital systems have always been appealing research topics. In this article, we present a useful trick to make the implementation of a digital noncoherent frequency shift keying (FSK) demodulator more economical from a hardware complexity standpoint, with the goal of minimizing its computational workload.

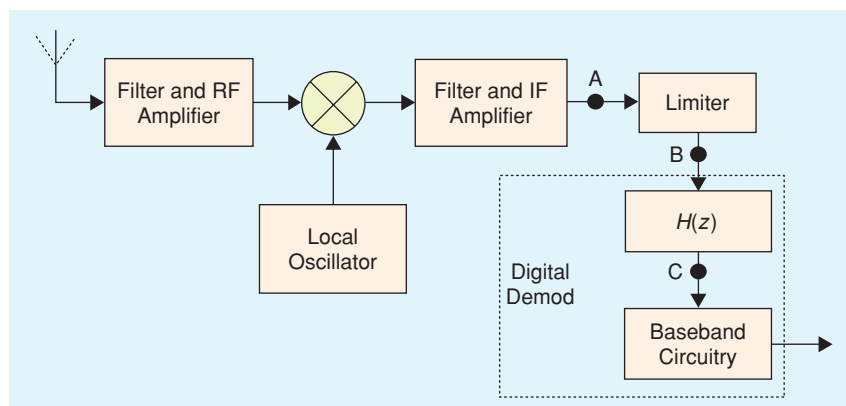
The RF front-end of a wireless receiver, shown in Figure 1, is mainly designed using analog components. Since the information of a noncoherent FSK signal is conveyed at zero-crossing points during each bit period, one often uses a limiter rather than an analog-to-digital converter (ADC) for the sake of hardware simplicity; the output of a limiter contains only two states and functionally behaves as a 1-b ADC. Thus, the signal at node B is a sequence of ones and zeros [1]. In the following, we shall call the signal at node A the intermediate-frequency (IF) signal.

Although a variety of receiver architectures (e.g., low IF and zero IF receivers) exist, we use the superheterodyne system as an example [2]. Owing to fabrication variation, the duty cycle of the IF signal is frequently not equal to 50% [2], [3]. That

is, the time duration of pulse “1” is not equal to that of pulse “0.” The curve in Figure 2(a) shows our analog IF signal, and the discrete samples in the figure show the binary sequence at the output of the limiter (node B in Figure 1).

In our application, the f_s sampling frequency of the digital demodulator is 10 MHz; the IF signal is located at frequency $f_1 = 455$ kHz; the frequency deviation f_D is set to ± 4 kHz; the data rate R is set to 4 kb/s; and a 30% duty cycle is assumed. The signal assumed in this example has a modulation index of 2 (i.e., $|2f_D/R| = 2$) so that the best bit error rate (BER) performance may be achieved for many popular FSK demodulators [4].

Examining the spectra of limiter output sequences in Figure 2(b) shows that there are harmonics located at integral multiples of $f_1 = 455$ kHz. In addition to those harmonics, there is a very large dc bias (0 Hz spectral component) on the limiter output signal that must be eliminated. The primary DSP trick in this article is to use a comb filter to solve this dc bias (dc offset) problem that, in addition, will also help us filter the limiter output signal's harmonics.



[FIG1] A noncoherent FSK demodulator preceded by a limiter and RF front-end circuitry.

“DSP Tips and Tricks” introduces practical tips and tricks of design and implementation of signal processing algorithms so that you may be able to incorporate them into your designs. We welcome readers who enjoy reading this column to submit their contributions. Contact Associate Editors Rick Lyons (r.lyons@ieee.org) or Amy Bell (abell@vt.edu).

USING A COMB FILTER

The comb filter we use to eliminate the dc bias, and minimize follow-on filter complexity, is the standard N -delay comb filter shown in Figure 3(a) [5]. Its periodic passbands and nulls are shown in Figure 3(b) for $N = 8$.

The z -domain transfer function of K cascaded comb filters is

$$H(z) = (1 - z^{-N})^K, \quad (1)$$

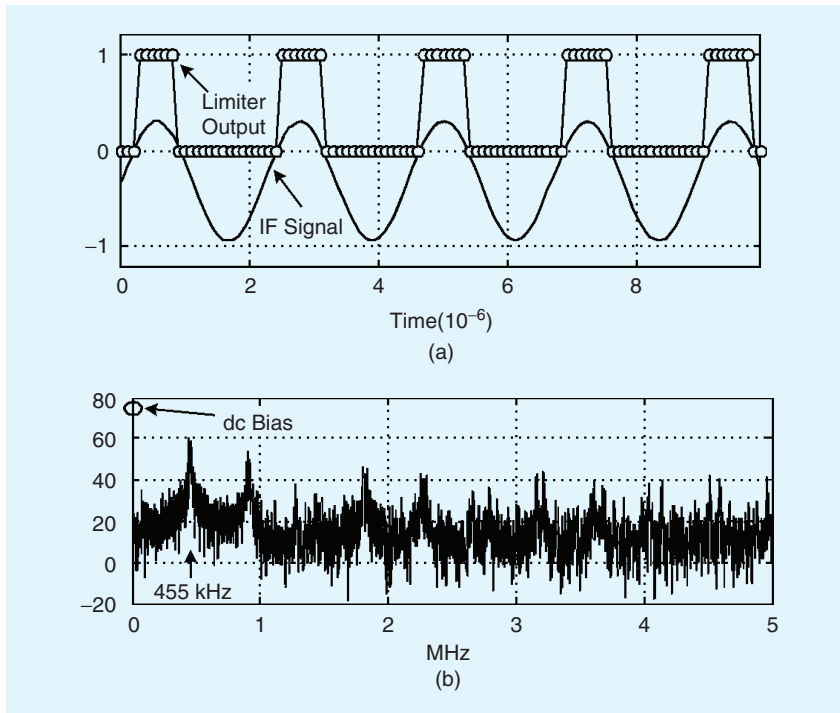
where in our application $K = 1$.

The following two equations allow us to locate the local minimum (L_{\min}) and local maximum (L_{\max}) in the positive-frequency range of $|H(\omega)|$:

$$L_{\min} : \omega = \frac{2\pi}{N} \cdot i, \quad i = 0, 1, \dots, \left\lfloor \frac{N}{2} \right\rfloor \quad (2)$$

$$L_{\max} : \omega = \frac{\pi}{N} + \frac{2\pi}{N} \cdot i, \quad i = 0, 1, \dots, \left\lfloor \frac{N-1}{2} \right\rfloor, \quad (3)$$

where $\lfloor q \rfloor$ means the integer part of q . Notice that these results are valid only for $N \geq 2$. If we regard the locations of L_{\max} as passbands and treat L_{\min} as stop-



[FIG2] Limiter signals: (a) limiter IF input and binary output and (b) output spectrum.

bands of $H(z)$, the comb filter can be viewed as a multiband filter.

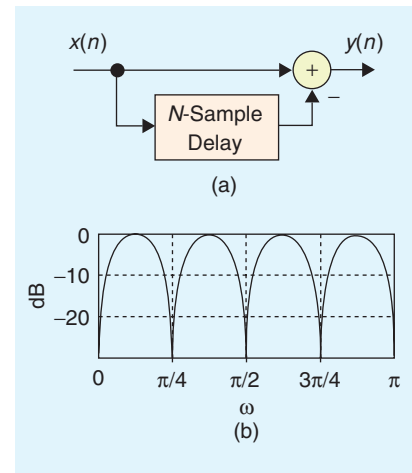
In general, the coefficient for each tap of an FIR filter is in floating-point format. Thus, multipliers and adders are generally required to perform signal filtering. However, $H(z)$ needs no multiplier and requires only an adder and a few registers. If the input sequence to such a filter is binary, as in our application, the adder of the comb filter becomes a simple XOR logic operation!

If there exists unwanted interference near dc, we may use multiple comb filters in cascade to further suppress these interfering signals. This may occur when low-frequency noise is present. However, the price paid in this case is nontrivial adders and multipliers. Some approaches have been proposed to simplify the hardware [6].

If the parameter N is carefully chosen such that $2\pi f_1/f_s$ is located at the first L_{\max} of the comb filter's magnitude response, all harmonics located at even multiples of f_1 and the 0 Hz (dc) component of the hard-limited signal applied to the comb filter can be suppressed. This operation is very helpful in reducing the hardware complexity of

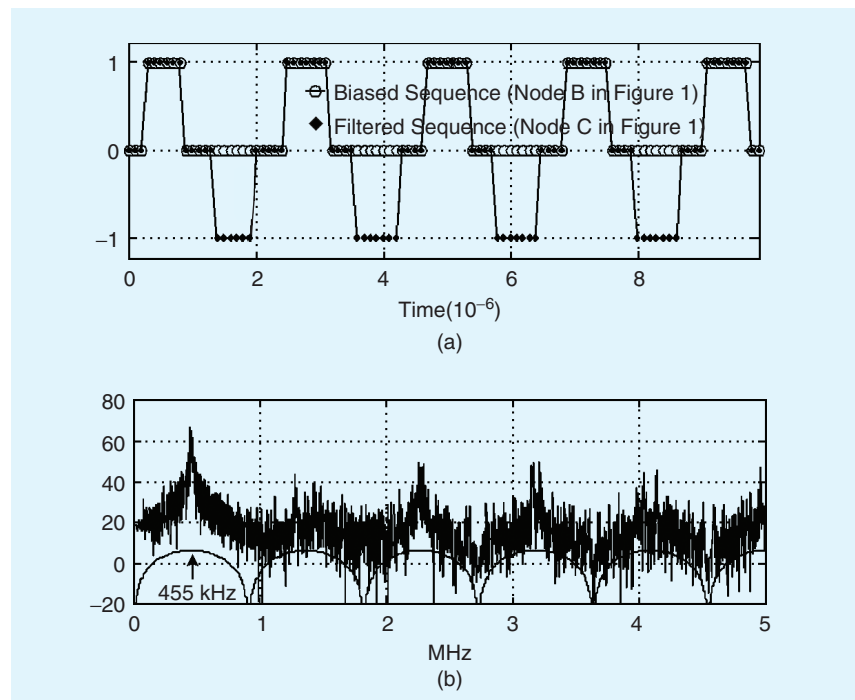
the following circuitry and enhancing the system performance of the noncoherent FSK receiver.

The signals into and out of the $H(z)$ comb filter, when $N = 11$, are shown in Figure 4(a). Examining the spectra of

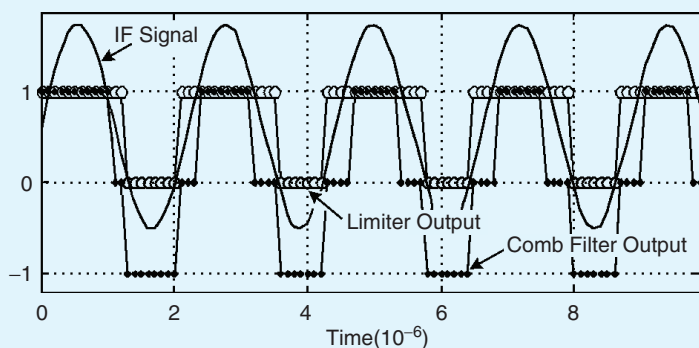


[FIG3] An $N = 8$ comb filter: (a) structure; (b) response $|H(\omega)|$.

the filtered output signal in Figure 4(b), we find that only our signal of interest at 455 kHz and odd harmonics of the fundamental frequency f_1 exist. For reference, the comb filter's $|H(\omega)|$ is shown in Figure 4(b). Since no low-frequency interference is assumed, we use $H(z)$, whose frequency response is superimposed in Figure 4(b) to suppress the dc offset of the IF signal. Comparing Figures 2(b) and 4(b), it is found that even harmonics and the dc component of the input signal are all diminished to



[FIG4] DC component removal for a binary IF signal using $H(z)$ with $N = 11$.



[FIG5] Limiter output signal at 60% duty cycle and $N = 11$ comb filter output.

a negligible degree. The odd harmonics are attenuated by follow-on filters where their computational workload is reduced because of the comb filter. Note that this efficient comb filtering also works for an M-ary FSK signaling by properly choosing the system parameters (e.g., f_L , f_s , f_D , R , and N).

BENEFICIAL COMB FILTER BEHAVIOR

The locations of the comb filter output harmonics remain unchanged even if the duty cycle of the blue sequence in Figure 2(a) changes. The length of the comb filter (N) is determined only by the sampling frequency f_s of the digital system and the IF frequency f_L . This fact, which is not at all obvious at first glance, means that our comb filter trick is inherently immune to the varying peak-to-peak amplitudes or changing dc bias levels of the analog IF signal that occur in many practical applications. To demonstrate this favorable comb filter behavior, let us assume the bias level (the average) of the analog IF signal in Figure 2(a), increased to a positive value such that the limiter's binary output sequence had a duty cycle of 60% as shown in Figure 5. Here we see how our $N = 11$ comb filter's output sequence is bipolar (dc bias removal has occurred), maintains a 50% duty cycle, and has a fundamental frequency equal to that of the IF signal.

A comb filter may also be used at the baseband to solve the same dc bias removal problem at demodulator output. Unlike that in the IF signal, the dc offset at demodulator output is a consequence of uncorrected frequency drift between

the transmitter and the receiver [7]. Thus, we can effectively combat variation in the bit duration of the demodulated data caused by the dc offset, which occurred in the baseband circuitry using the same methodology.

SUMMARY

In this article, we showed how an efficient comb filter can be used to both remove the dc offset from our signals and reduce the complexity of follow-on filtering. The advantages of the comb filter are its implementation simplicity (a single exclusive-OR circuit) and its ability to combat the problem of dc offset for both IF and baseband signals. Through examples, we showed that the duty cycle for signals at the IF can be easily corrected to a 50% duty cycle. This corrected signal is amenable to additional processing at its IF frequency or may be down-converted to a baseband frequency for further processing.

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CORRECTION

In the January issue of *IEEE Signal Processing Magazine*, in the "DSP History" column, the name "M.M. Londhi" is incorrect; the correct name is "M.M. Sondhi."

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